

CLAIMS

1. An image reject circuit comprising:

5 a local oscillator for producing a local oscillator signal;

a tunable phase shifting network for receiving the local oscillator signal and producing an output in-phase (I) signal and an output quadrature (Q) signal;

10 a first amplitude detector for determining the amplitude of the output I signal;

a second amplitude detector for determining the amplitude of the output Q signal; and,

15 means for determining the difference between the amplitudes of the output I and Q signals, to produce a tuning signal for tuning the phase shifting network to bring the difference between the amplitudes of the output I and Q signals towards a desired level.

20 2. An image reject circuit as claimed in claim 1, wherein the phase shifting network has first and second input terminals for receiving the local oscillator signal, and comprises:

25 a first phase shifting circuit connected between the first input terminal and a voltage reference;

30 a second phase shifting circuit connected between the voltage reference and the second input terminal;

first and second pairs of complementary output lines connected to each of the first and second phase shifting circuits; and,

35 a tuning input for receiving a tuning signal.

3. An image reject circuit as claimed in claim 2, wherein each of the first and second phase shifting circuits comprises a bridge circuit, each bridge circuit comprising:
- 5 first and second parallel arms connected between the respective input terminal and the voltage reference;
- the first arm comprising a resistive element connected in series with a capacitive element;
- 10 the second arm comprising a capacitive element connected in series with a resistive element; and,
- each I and Q output line being connected to a respective junction between the series connected resistive element and capacitive element.
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4. An image reject circuit as claimed in any one of claims 1 to 3, wherein ~~the~~ phase shifting network is tuned by adjusting an RC time constant.
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5. An image reject circuit as claimed in claim 4, wherein the capacitive element comprises a reverse polarity junction diode, which is tuned in accordance with the tuning signal.
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6. An image reject circuit as claimed in claim 4, wherein the resistive element comprises a variable resistor, which is tuned in accordance with the tuning signal.
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7. An image reject circuit as claimed in claim 4, wherein the resistive element comprises a variable resistor, the capacitive element comprises a reverse polarity junction diode, both of which are tuned in accordance with the tuning
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signal.

8. An image reject circuit as claimed in claim 6 or 7, wherein the resistive element comprises a MOSFET operated in its triode region.

9. An image reject circuit as claimed in claim 2, wherein each of the first and second phase shifting circuits comprises a bridge circuit, each bridge circuit comprising:

first and second parallel arms connected between the respective input terminal and the voltage reference;

the first arm comprising a resistive element connected in series with an inductive element;

the second arm comprising an inductive element connected in series with a resistive element;

each I and Q output line being connected to a respective junction between the series connected resistive element and inductive element;

wherein the phase shifting network is tuned by adjusting the RL time constant.

10. An image reject circuit as claimed in claim 2, wherein each of the first and second phase shifting circuits comprises a bridge circuit, each bridge circuit comprising:

first and second parallel arms connected between the respective input terminal and the voltage reference;

the first arm comprising an inductive element connected in series with a capacitive element;

the second arm comprising a capacitive element connected in series with an inductive

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15. An image reject circuit as claimed in claim 14, further comprising a limiting stage for removing any residual difference between the

amplitudes of the I and Q signals.

16. An image reject circuit as claimed in claim
14 or 15, further comprising an RC poly-phase
filter section for removing any residual
difference between the amplitudes of the I and Q
signals.
17. An image reject circuit as claimed in any one
of claim 1 to 13, wherein the desired difference
between the amplitudes of the output I and Q
signals is set to a predetermined level, to
compensate for an amplitude error found elsewhere
in the system.
18. An image reject circuit as claimed in any one
of the preceding claims, wherein the circuitry is
implemented in bipolar technology.
19. An image reject mixer as claimed in any one
of claims 1 to 17, wherein the circuitry is
implemented in CMOS, BiCMOS, SiGe or GaAs
technology.
20. An image reject circuit as claimed in any one
of the preceding claims, wherein the circuit is
implemented as an integrated circuit.
21. An image reject circuit as claimed in any
preceding claim, further comprising a second
tunable phase shifting network located in an
intermediate frequency path, the tuning signal of
the first phase shifting network also being used
to tune the second phase shifting network.

22. A method of rejecting images in a receiver circuit comprising a local oscillator for producing a local oscillator signal, and a tunable phase shifting network for receiving the local oscillator signal and producing an output in-phase (I) signal and an output quadrature (Q) signal, the method comprising the steps of;

determining the amplitude of the output I signal;

determining the amplitude of the output Q signal;

determining the difference between the amplitudes of the output I and Q signals, to produce a tuning signal; and,

using the tuning signal to tune the phase shifting network to bring the difference between the amplitudes of the output I and Q signals towards a desired level.

23. A method as claimed in claim 22, wherein the phase shifting network is tuned by adjusting an RC time constant of the phase shifting network.

24. A method as claimed in claim 23, wherein the RC time constant is changed by changing the voltage across junction diodes, the change in voltage causing the capacitance of the junction diodes to change accordingly.

25. A method as claimed in claim 23, wherein the RC time constant is changed by changing the resistance value of a variable resistor

26. A method as claimed in claims 23, wherein the RC time constant is changed by changing the

capacitance value and the resistance value.

27. A method as claimed in claim 25 or 26,
wherein the resistance value is changed by
operating a MOSFET in its triode region.

28. A method as claimed in claim 22, wherein the
phase shifting network is tuned by adjusting an RL
time constant of the phase shifting network.

29. A method as claimed in claim 22, wherein the
phase shifting network is tuned by adjusting an LC
time constant of the phase shifting network.

30. A method as claimed in any one of claims 22
to 29, wherein the amplitudes of the I and Q
signals are determined using amplitude detectors.

31. A method as claimed in any one of claims 22
to 30, in which the receiver further comprises a
second tunable phase shifting network located in
an intermediate frequency path, the method
comprising the further step of tuning the second
phase shifting network according to the tuning
signal determined for the first phase shifting
network.

32. A method as claimed in any one of claims 22
to 31, wherein the phase shifting network is tuned
such that the desired difference between the
amplitudes of the I and Q signals is substantially
zero.

33. A method as claimed in any one of claims 22
to 32, wherein the phase shifting network is tuned

such that the desired difference between the amplitudes of the output I and Q signals is set to a predetermined level, to compensate for an amplitude error found elsewhere in the system.

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34. A tunable phase shifting network for use in an image reject circuit, the tunable phase shifting network comprising:

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first and second input terminals for receiving an input signal;

a first phase shifting circuit connected between the first input terminal and a voltage reference;

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a second phase shifting circuit connected between the voltage reference and the second input terminal;

wherein each phase shifting circuit comprises:

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first and second parallel arms connected between the respective input terminal and the voltage reference;

the first arm comprising a resistive element connected in series with a capacitive element;

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the second arm comprising a capacitive element connected in series with a resistive element; and,

I and Q output lines being connected to respective junctions between the series connected resistive element and capacitive element; and,

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wherein the phase shifting network further comprises a tuning input for receiving a tuning signal for adjusting an RC time constant of the phase shifting network.

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35. A tunable phase shifting network as claimed

in claim 34, wherein the capacitive element comprises a reverse polarity junction diode, which is tuned in accordance with the tuning signal.

5 36. A tunable phase shifting network as claimed in claim 34, wherein the resistive element comprises a variable resistor, which is tuned in accordance with the tuning signal.

10 37. A tunable phase shifting network as claimed in claim 34, wherein the resistive element comprises a variable resistor, the capacitive element comprises a reverse polarity junction diode, both of which are tuned in accordance with
15 the tuning signal.

38. A tunable phase shifting network as claimed in claim 36 or 37, wherein the resistive element comprises a MOSFET operated in its triode region.

20 39. A tunable phase shifting network for use in an image reject circuit, the tunable phase shifting network comprising:

25 first and second input terminals for receiving an input signal;

 a first phase shifting circuit connected between the first input terminal and a voltage reference;

30 a second phase shifting circuit connected between the voltage reference and the second input terminal;

 wherein each phase shifting circuit comprises:

35 first and second parallel arms connected between the respective input terminal and the

voltage reference;

the first arm comprising a resistive element connected in series with an inductive element;

the second arm comprising an inductive element connected in series with a resistive element; and,

I and Q output lines being connected to respective junctions between the series connected resistive element and inductive element; and,

wherein the phase shifting network further comprises a tuning input for receiving a tuning signal for adjusting an RL time constant of the phase shifting network.

40. A tunable phase shifting network for use in an image reject circuit, the tunable phase shifting network comprising:

first and second input terminals for receiving an input signal;

a first phase shifting circuit connected between the first input terminal and a voltage reference;

a second phase shifting circuit connected between the voltage reference and the second input terminal;

wherein each phase shifting circuit comprises:

first and second parallel arms connected between the respective input terminal and the voltage reference;

the first arm comprising an inductive element connected in series with a capacitive element;

the second arm comprising a capacitive element connected in series with an inductive element; and,

I and Q output lines being connected to respective junctions between the series connected inductive element and capacitive element; and,

5 wherein the phase shifting network further comprises a tuning input for receiving a tuning signal for adjusting an LC time constant of the phase shifting network.